AN-SM2306

POWERMASTER SEMICONDUCTOR
Masters of Power Solution

Fast Recovery SJ MOSFET, *e*MOS F7 Technology for Resonant Topologies

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1. Introduction

Resonant topologies are essentially block for high efficiency and bi-directional operation in many applications. 600V / 650V eMOS F7 series is Power Master Semiconductor's latest high voltage super-junction technology with integrated fast body diode. eMOS F7 series has a low reverse recovery charge (Q_{RR}) and robust body diode performance. 600V / 650V eMOS F7 series is developed to provide optimized solution for resonant topologies and bridge topologies that required high efficiency, high power density and high system reliability for various power conversion systems such as consumer, industrial and automotive applications. This application note will describe optimized characteristics of eMOS F7 series for resonant topologies.

1.1. What is super-junction MOSFET?

The major contribution to $R_{DS(ON)}$ of high-voltage MOSFET (>500V) comes from the epi layer, The portion of epi resistance is higher for high breakdown voltage MOSFETs due to the higher resistivity or lower carrier concentration in the epi layer. Therefore, epi resistance should be decreased for the lower $R_{DS(ON)}$·Q_G, Figure of Merit(FOM) for high voltage MOSFETs. The super-junction technology utilizing charge balance technology is widely using for high voltage Si MOSFETs to overcome silicon limitation. Figure 1 shows vertical structure and electric field profile of a conventional planar MOSFET and super-junction MOSFET. Breakdown voltage of the planar MOSFET is determined by drift doping and its thickness. The slope of electric field distribution is proportional to drift doping. Therefore, thick and lightly doped epi is needed to support higher breakdown voltage. Super-junction technology has long p-type pillar structure in the body. The effect of the p-type pillars is to confine the electric field in the lightly doped epi region. Therefore, super-junction technology can increase breakdown voltage with same doping and epi thickness by larger electric field area thanks to p-type pillar in figure 1. In other words, a much lower specific on-resistance can be achieved with super-junction structures by increasing the N-drift dose while maintaining same breakdown voltage.

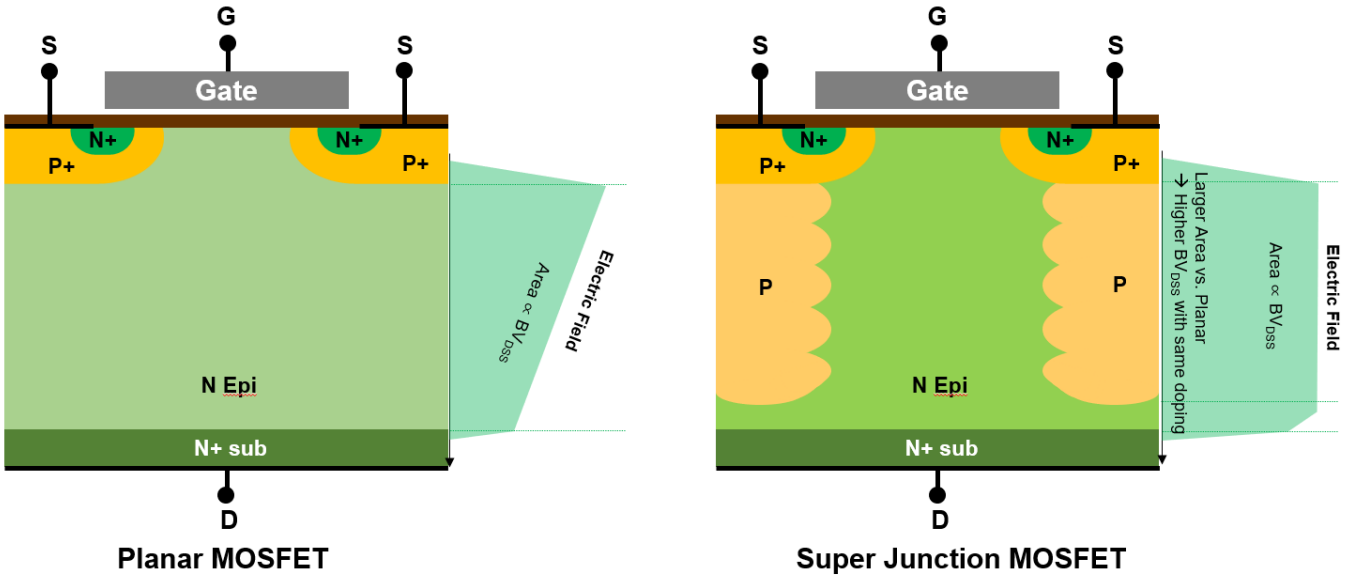


Figure 1. Vertical structure and electric field profile : planar MOSFET vs super-junction MOSFET

2. 600V / 650V eMOS F7 Technology

2.1. Target Applications

As shown in figure 2, The eMOS F7 series is designed to achieve excellent performance especially in resonant topologies and bridge topologies for various applications such as TV powers (LCD / LED / OLED), server / telecom powers, PV inverters, EV chargers for DC EV charging piles (EVC) and on-board chargers (OBC).

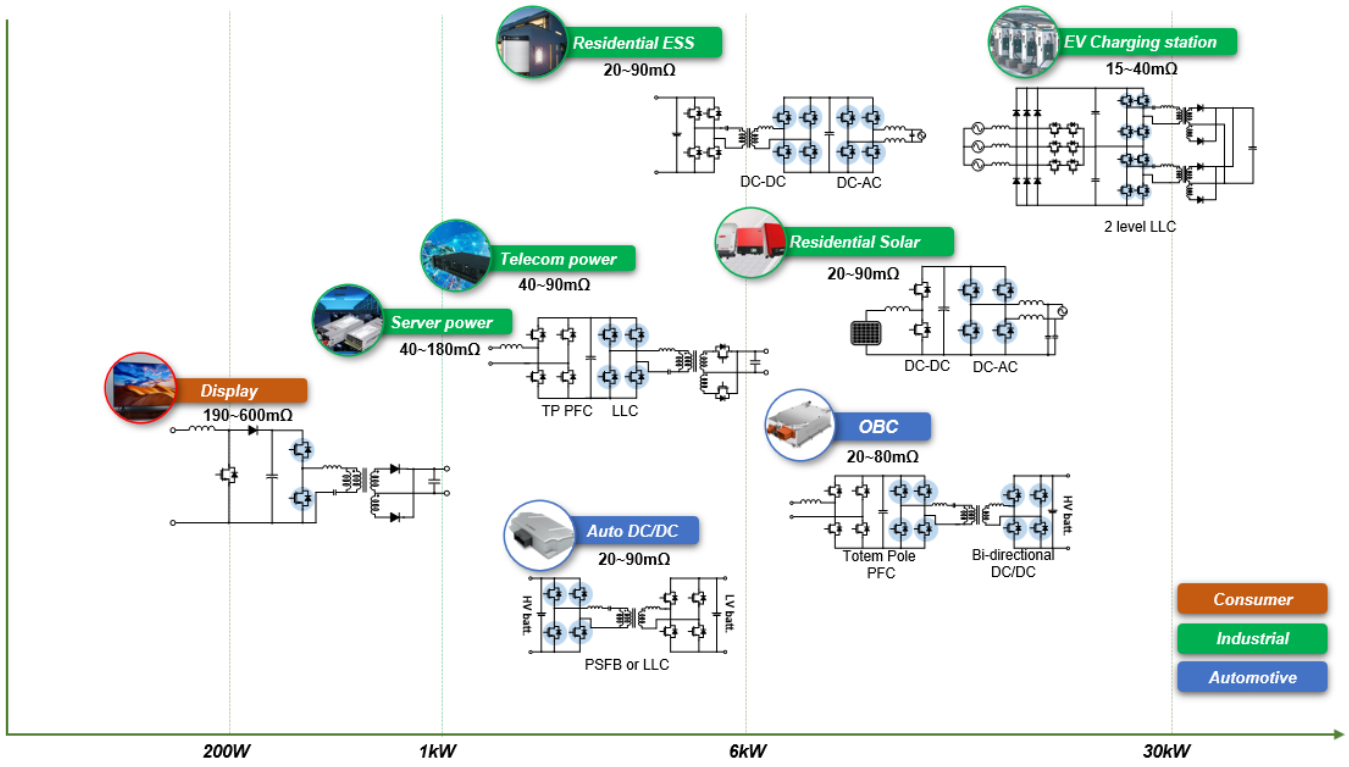


Figure 2. 600V / 650V eMOS F7 Series - Target applications

2.2. 600V / 650V eMOS F7 – Features and Benefits

The target performance of 600V / 650V eMOS F7 series is to combines fast switching and high performance of body diode. Therefore, 600V / 650V eMOS F7 provides higher reliability for resonant topologies such as LLC resonant converters or phase shifted full bridge converters. It enables to offer high performance and robust solution with a wide range of package options. As shown in figure 3, The 600V / 650V eMOS F7 series has highly optimized key performance for primary switch of soft switched LLC resonant topologies or phase shifted full bridge topologies.

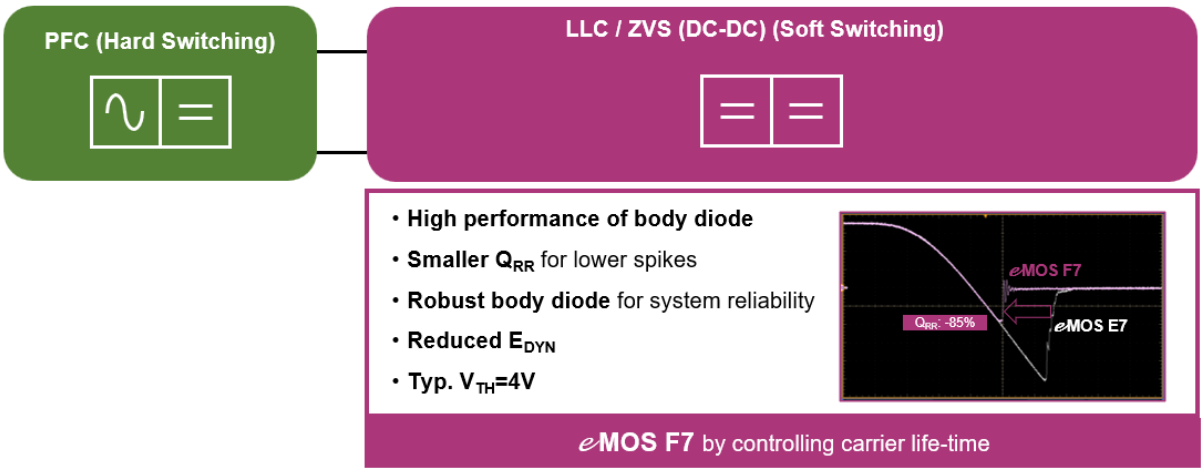


Figure 3. eMOS F7's optimized performance for soft switching topologies

The 600V / 650V eMOS F7 is an advanced Power Master Semiconductor's super-junction MOSFET family by utilizing charge balance technology and life-time killing process for both excellent low on-resistance and body diode performance. This technology combines the benefits of fast switching performance with low Q_{RR} of body diode and robustness. Robust integrated body diode performance of 600V / 650V eMOS F7 provide better reliability in soft switching topologies during abnormal operation such as start-up and output short circuit mode.
Consequently, the eMOS F7 family is well-optimized for many applications requiring higher efficiency and higher system reliability.

Key Features

- Excellent body diode performance - Smaller Q_{RR}
- Improved body diode dv/dt and di/dt ruggedness
- Lower E_{DYN}

Key Benefits

- Suitable for soft switching (LLC)
- Highest reliability for resonant topologies
- High light load efficiency.
- Suitable for a wide variety of applications and power ranges

2.3. 650V eMOS F7 – Key Electrical Characteristics

The key electrical parameters of 650V eMOS is compared to those of three competitor's fast recovery super-junction MOSFETs. Power Master Semiconductor's the fast recovery super-junction MOSFET, 650V eMOS F7 has very competitive performance against competitor's fast recovery super-junction MOSFETs.

Table 1 shows the key parameter comparison of Power Master Semiconductor's 650V/43mΩ, TO-247, eMOS F7 and the competitor's fast recovery super-junction MOSFETs. 650V eMOS F7 shows the lowest E_{OSS} and dynamic capacitance loss (E_{DYN}) that is critical factor for efficiency in soft switching topologies with very competitive FOMs against competitors and guarantee high peak diode recovery dv/dt (50V/ns) for better system design margin.

Table 1. Key parameter comparison of Power Master Semiconductor's 650V/43mΩ eMOS F7 and the competitor.

Specification	PMW65N043F7	Comp. A	Comp. B	Comp. C
BV_{DSS}	650 V	650 V	650 V	650 V
I_D	64 A	68.5 A	65 A	80 A
I_{DM}	192 A	255 A	162.5 A	240 A
$R_{DS(on)}$ Max	43 mΩ	41 mΩ	40 mΩ	38 mΩ
*Q_G at V_{DD}=400V, I_D=32A, V_{GS}=0~10V	142 nC	280 nC	150 nC	172 nC
*Q_{RR} at V_{DD}=400V, I_D=32A, di/dt=100A/μs	1.4 μC	1.0 μC	1.0 μC	1.6 μC
*E_{OSS} at V_{DS}=400V	16.5 μJ	22.8 μJ	19.4 Ω	22.7 Ω
*Q_{OSS} at V_{DS}=400V	553 nC	548 nC	738 nC	619 nC
*E_{DYN} at V_{DS}=400V	6.5 μJ	9.4 μJ	9.1 μJ	6.0 μJ
FOM [$R_{DS(on)}$·Q_G]	6.1 Ω·nC	11.5 Ω·nC	6.0 Ω·nC	6.5 Ω·nC
FOM [$R_{DS(on)}$·E_{OSS}]	0.7 Ω·μJ	0.9 Ω·μJ	0.8 Ω·μJ	0.9 Ω·μJ
FOM [$R_{DS(on)}$·Q_{OSS}]	23.8 Ω·nC	22.5 Ω·nC	29.5 Ω·nC	23.5 Ω·nC
Peak Diode Recovery dv/dt	50 V/ns	50 V/ns	50 V/ns	50 V/ns

Note : "*" measured value at same test conditions

2.4. 650V eMOS F7 – Competitor Benchmark

Figure 4 shows the 650V eMOS F7 performance position against competitors. As shown in this spider chart, 650V eMOS F7 offers very low switching losses with the best-in-class E_{DYN} against competitor's fast recovery super-junction MOSFETs. 650V eMOS F7 has excellent FOMs. The low E_{DYN} of 650V eMOS F7 can reduce dynamic capacitance loss that is critical in soft switching topologies. Thanks to excellent body diode performance (low Q_{RR} and robust body diode ruggedness) of 650V eMOS F7 technology, it is optimized for resonant topologies such as ZVS phase-shifted full bridge or LLC resonant converters. 650V eMOS' F7's outstanding parameters result in the higher system efficiency and reliability in target applications.

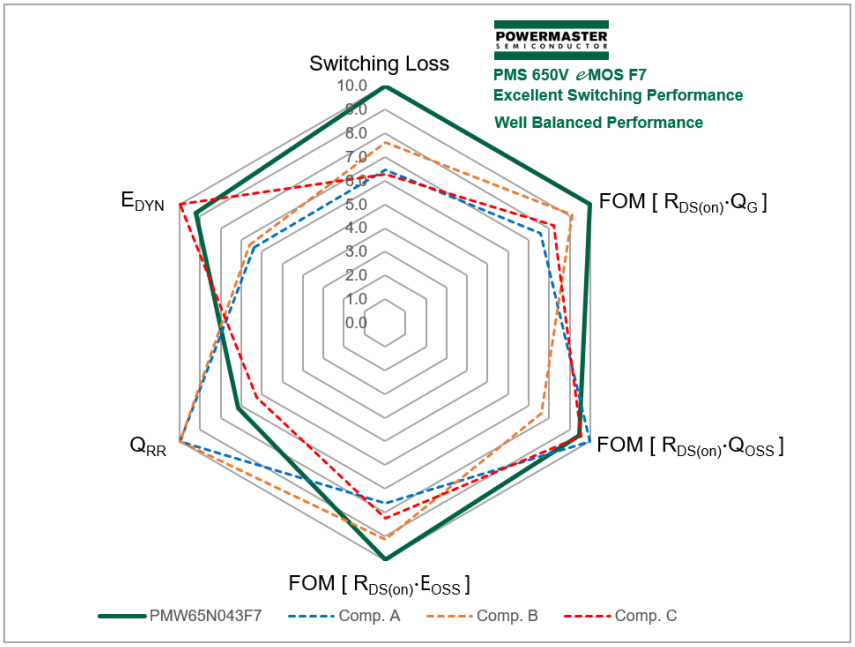
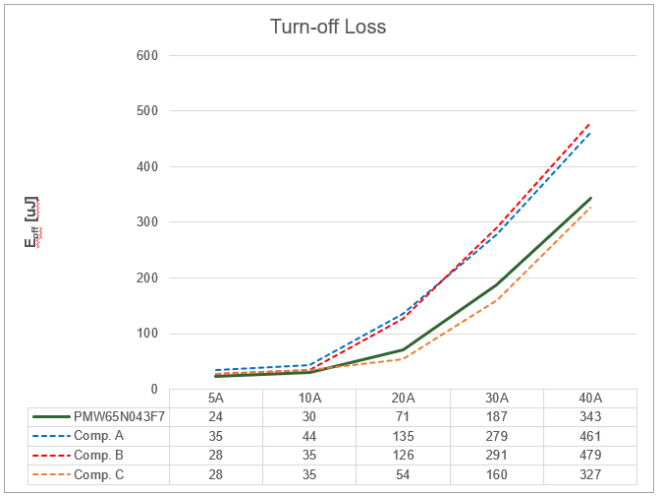


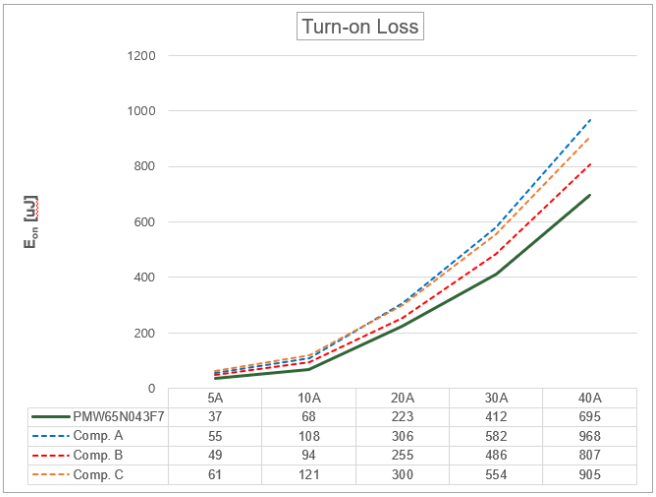
Figure 4. 650V/43mΩ *e*MOS F7 performance position against competitor's fast recovery SJ MOSFETs (Note1: 10 is the best, 0 is the worst)

2.5. 650V *e*MOS F7 – Switching Characteristics

Figure 5 shows switching losses (E_{ON} and E_{OFF}) comparison for 650V/43mΩ *e*MOS F7 vs competitors under same test conditions, V_{DD}=400V, I_D=5~40A, V_{GS}=10V, R_G=3Ω. Switching losses of 650V *e*MOS F7 are reduced compared to that of competitor's devices. As shown in figure 5, 650V/43mΩ *e*MOS F7 shows approximately 33~36% lower turn-off loss and 15~29% lower turn-on loss compared to competitors.



(a) Turn-on switching loss (E_{ON}) comparison



(b) Turn-off switching loss (E_{OFF}) comparison

Figure 5. 650V/43mΩ *e*MOS F7 switching loss comparison under V_{DD}=400V, I_D=2~20A, V_{GS}=10V, R_G=3Ω. at inductive load switching

3. Key Requirement Parameters in Resonant Topologies

3.1. Low E_{OSS} in Resonant Topologies

In LLC resonant topologies, the effective capacitance is used to ensure ZVS. Zero voltage turn-on is achieved by using the stored energy in inductor, the leakage and series inductance or magnetizing inductance of the transformer, to discharge the output capacitance of the primary switches through resonant action in figure 6.

The following equations are basic requirements for zero voltage switching.

Equation 1)

Inductive Energy ≥ Capacitive Energy

$$\frac{1}{2}\cdot \mathrm{L}_{eq}\cdot I_L^2 \geq \frac{1}{2}\cdot (2\cdot C_{OSS_{(er)}})\cdot V_{DS}^2 \qquad \frac{1}{2}\cdot \mathrm{L}_{eq}\cdot I_L^2 \geq 2\cdot \mathrm{E}_{OSS}$$

Where, $C_{OSS(er)}$ and E_{OSS} is energy related output capacitance and stored energy in C_{OSS} of Q_1 or Q_2 at input voltage.
L_{eq} is equivalent inductance in figure 6.

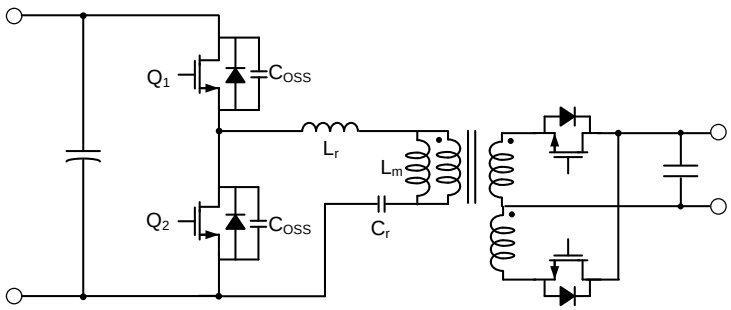


Figure 6. Half-Bridge LLC Resonant Converter

Zero voltage switching (ZVS) topologies can achieve lossless turn-on while drain-source voltage is zero by flowing current through the body diode during dead time as shown in figure 7. MOSFET output capacitance is crucial parasitic parameter to understand for zero voltage switching (ZVS) topologies. It determines how much inductance is required to provide ZVS conditions because MOSFET output capacitance can be used as a resonant component in soft switching topologies in equation 1. The inductance should be precisely designed to prevent hard switching that causes additional power losses. To achieve ZVS, the magnetizing current and dead time must be great enough to discharge the output capacitance of one MOSFET and charge another. If the inductive energy is too small, the circuit will operate in hard switching mode, losing some of the efficiency gained by changing to a resonant topology. If the inductive energy is too large, excess energy will be lost, again minimizing the efficiency gained through the using of a resonant topology. In order to design the resonant circuit such that the inductive energy is as low as possible while still maintaining ZVS as in equation 1.

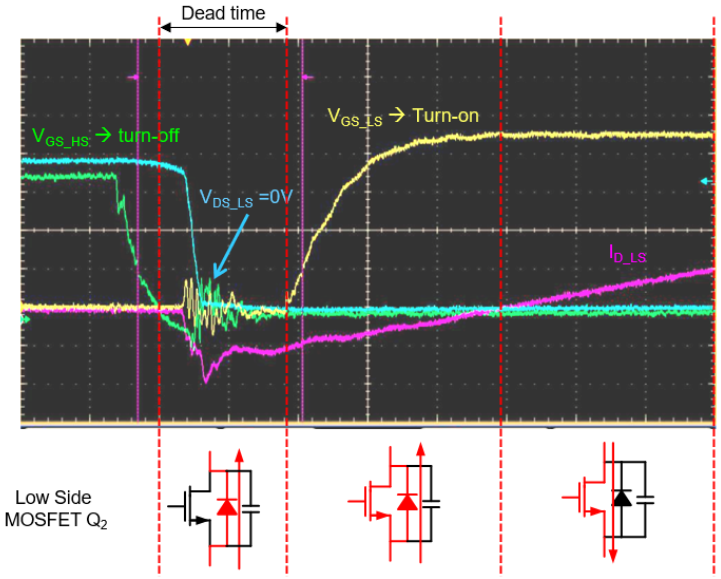


Figure 7. ZVS Operation Modes of Power MOSFET in LLC Resonant Converter

As shown in figure 8, 650V/43mΩ eMOS F7 has approximately 15~28% less stored energy in output capacitance than competitors. Therefore, eMOS F7 requires less energy to achieve ZVS operation.

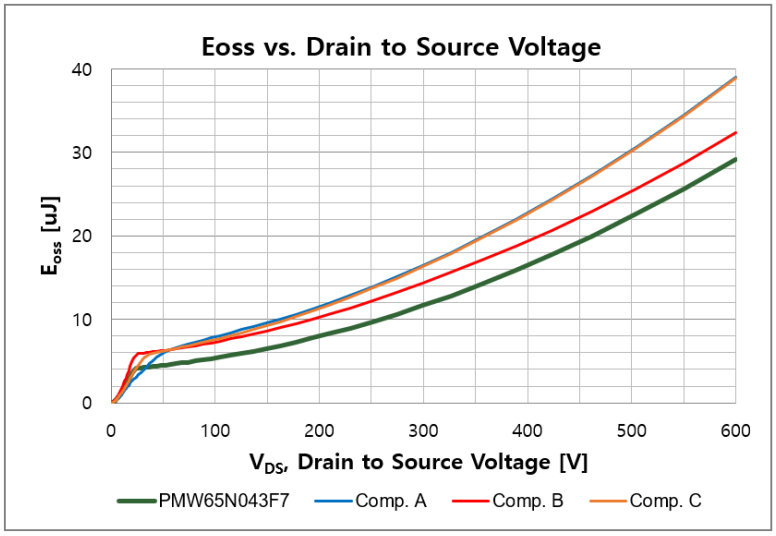


Figure 8. E_{OSS} Comparison of 650V/43mΩ eMOS F7 vs. competitor's fast recovery SJ MOSFETs

3.2. Low Q_{OSS} in Resonant Topologies

Q_{OSS} is the amount of charge for charging drain-source capacity. The reduction in Q_{OSS} is critical to achieve ZVS, the dead time between the high side and low side MOSFETs in the same leg must be long enough to allow the voltage transition. The time condition for achieving ZVS is given by equation 2.

Equation 2) Dead time condition for ZVS

$$\text{dead time} \geq 2 \cdot \frac{Q_{oss}}{I}$$

where I is the current used to charge and discharge both FETs in the leg

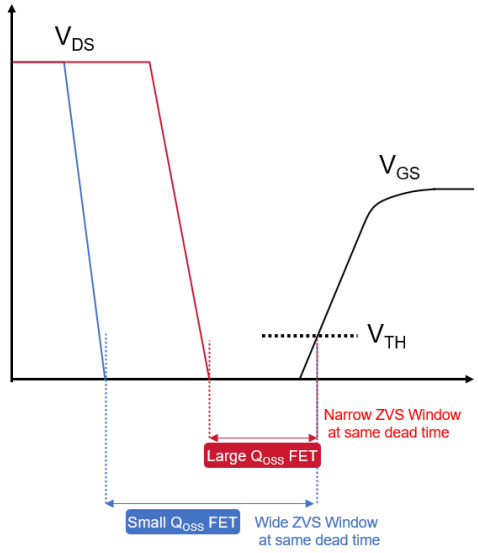


Figure 9. Dead time margin by Qoss

In resonant topologies, Qoss is directly related to the charge which has to be provided and also the time needed to build up or release the reverse voltage. As shown in figure 9, MOSFETs that have smaller Qoss provide wider ZVS window at same dead time than that has larger Qoss. As shown in figure 10, 650V/43mΩ eMOS F7 has approximately 11~25% less charge in output capacitance than competitors. Therefore, eMOS F7 enables less dead time and losses with its low Qoss.

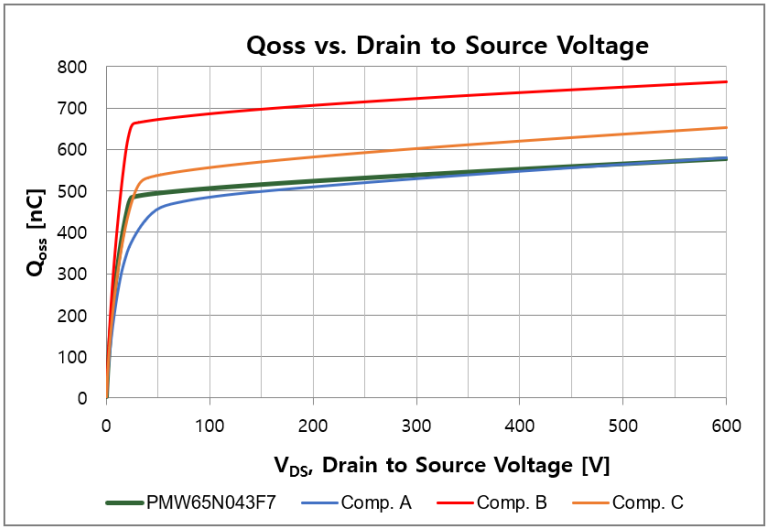


Figure 10. Qoss Comparison of 650V/43mΩ eMOS F7 vs. competitor's fast recovery SJ MOSFETs

3.3. Low dynamic C_{OSS}, E_{DYN} in Resonant Topologies

Dynamic C_{OSS} (E_{DYN}) is power losses associated with the super junction MOSFETs in ZVS topologies generated. When the MOSFET C_{OSS} is charged and subsequently discharged some energy is lost due to the hysteretic phenomenon that the entire energy stored in the output capacitance (E_{OSS}) is not recovered. E_{DYN} can be observed by hysteresis loop area large signal C_{OSS} during charge-discharge cycle as shown in figure 11.

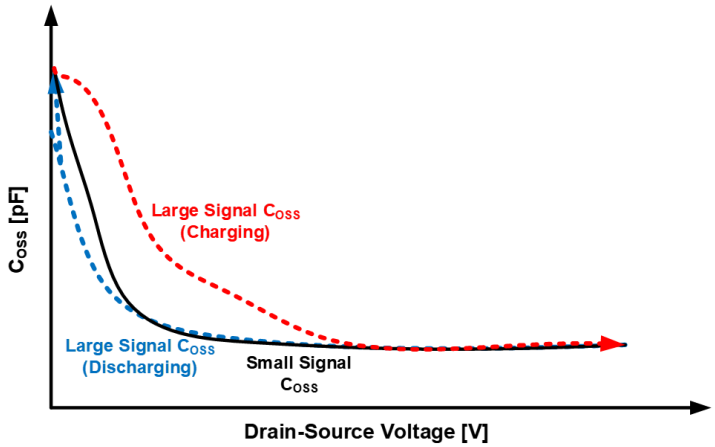


Figure 11. Comparison between small signal C_{OSS} (black line) and large signal C_{OSS}(red and blue lines)

The energy loss (E_{DYN}) related to dynamic C_{OSS} of the super-junction MOSFET depends on the device structure, die size, switching dV_{DS}/dt. A dynamic C_{OSS} loss (E_{DYN}) generates for every switching cycle and increases the energy dissipated in the device. Resonant converters are supposed to generate zero switching losses during soft switching operation, Dynamic C_{OSS} loss (E_{DYN}) is highly impact on system efficiency especially, in resonant topologies at light load and high switching frequency operation. As shown in figure 12, 650V/43mΩ eMOS F7 has approximately 29~31% less dynamic C_{OSS} loss (E_{DYN}) than competitors. Therefore, eMOS F7 provides higher system efficiency in LLC resonant topologies by its lower E_{DYN}.

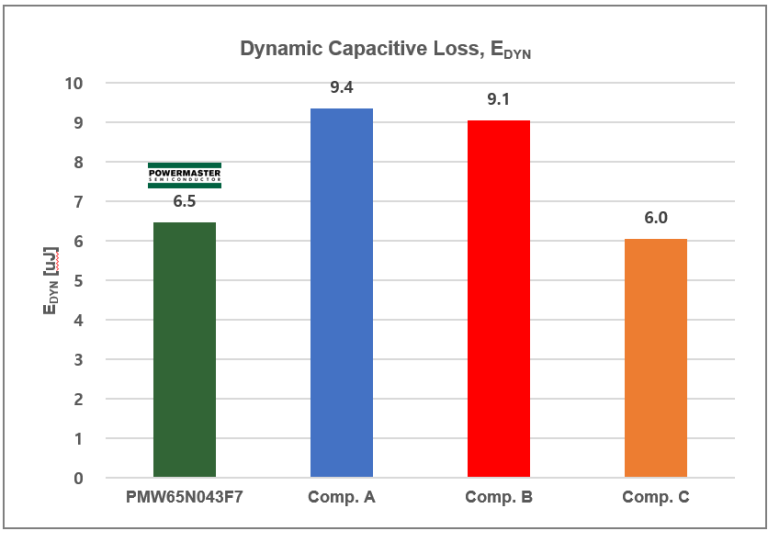


Figure 12. E_{DYN} Comparison of 650V/43mΩ eMOS F7 vs. competitor's fast recovery SJ MOSFETs

3.4. Body Diode Ruggedness in Resonant Topologies

In LLC resonant converter, poor body diode performance of primary MOSFETs can lead to some unexpected system or device failures associated with severe shoot-through current, body diode dv/dt, breakdown dv/dt, and gate oxide breakdown in various abnormal conditions such as start-up, load transient, and output short circuit. During start-up, the ZVS operation can be lost and MOSFETs can fail due to reverse recovery dv/dt. Resonant capacitance and output capacitance are completely discharged before start-up. These empty capacitances cause further conduction of Q_2 body diode and it is not recovered completely before Q_1 turns on in figure 6. This reverse recovery current is very high and is enough to make shoot-through problems during start-up, as shown in figure 13.

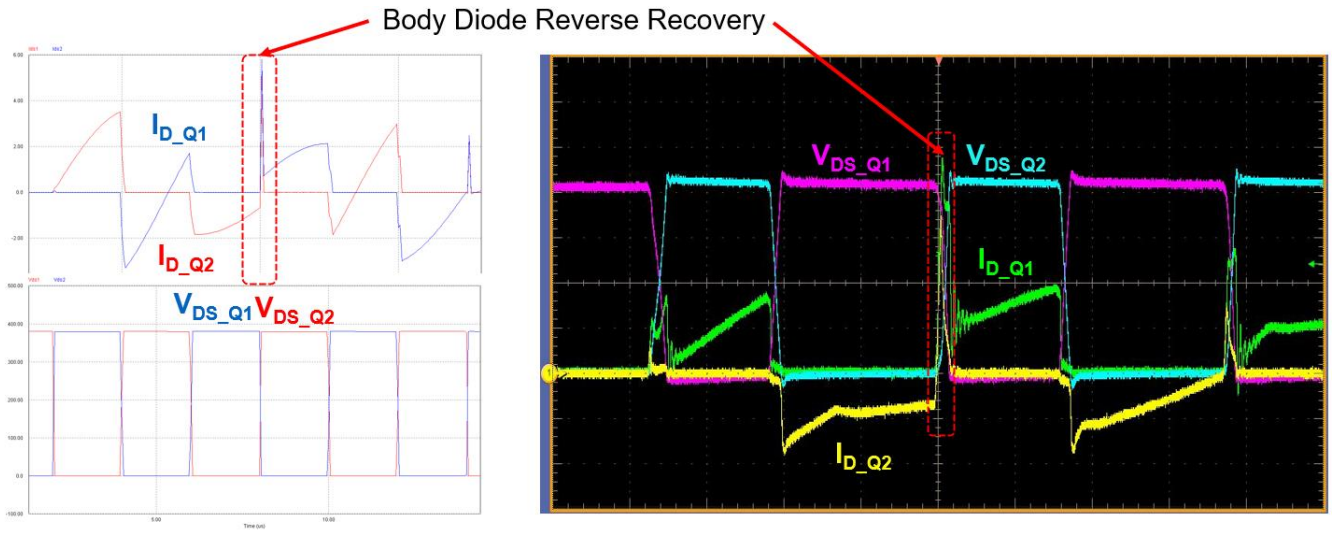


Figure 13. Waveforms during start-up in the LLC resonant converter (left : simulation, right : measurement)

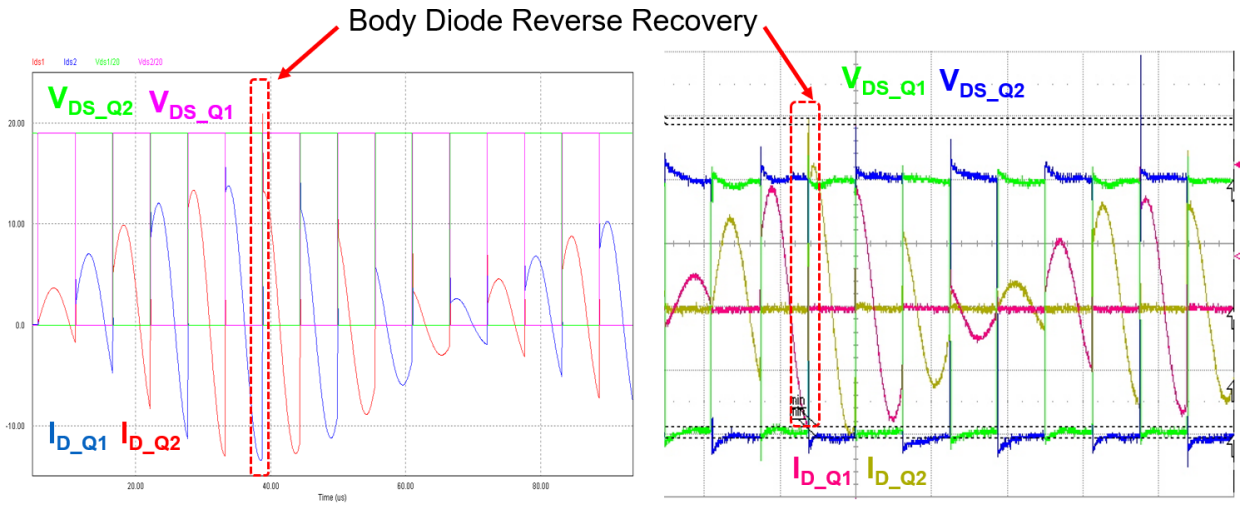


Figure 14. Waveforms during output short in the LLC resonant converter (left : simulation, right : measurement)

During the output short mode, the MOSFET conducts an extremely high current. When the output short circuit occurs, L_m is shunted in resonance. The LLC resonant converter can be simplified as a series resonant tank by C_r and L_r because C_r resonates with only L_r in figure 6. This condition usually results in the ZCS operation (capacitive mode). The most severe drawback of the ZCS operation is hard commutation at turn-on, which can lead to the diode reverse recovery stress (dv/dt) and huge current and voltage stress as shown in figure 14. Also, the device or system can be damaged by gate over voltage stress because of the high di/dt and dv/dt during its body diode reverse recovery as shown in figure 15.

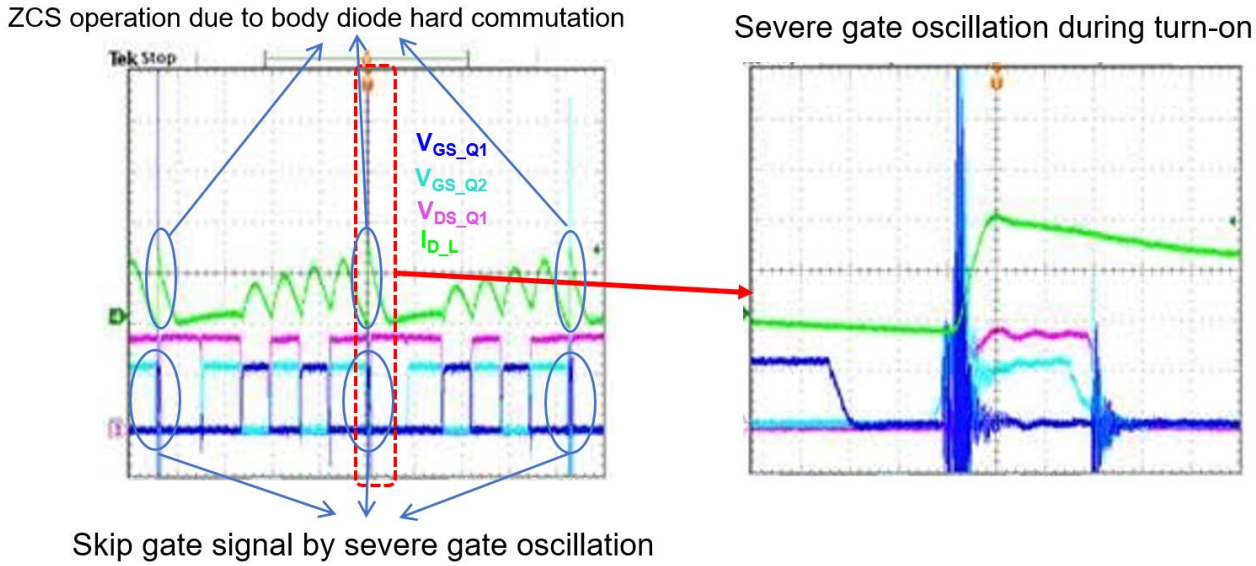


Figure 15. Severe gate oscillation during output short in the LLC resonant converter

Replacing a normal MOSFET with a fast recovery MOSFET (eMOS F7) is the most simple and effective to implement because additional circuits or components are not necessary. Figure 16 shows an improvement of reverse recovery characteristics of a fast recovery eMOS F7 compared to a normal MOSFET, eMOS E7. The reverse recovery charge of the eMOS F7 is reduced by 90% compared to eMOS E7. The body diode ruggedness of the eMOS F7 is much better than a normal MOSFET. In addition, the peak gate-source voltage of low-side MOSFET can decrease from 54V to 25V when devices changed to eMOS F7 from eMOS E7 during reverse recovery operation by reduced Q_{RR}. With all of these improved characteristics, eMOS F7 provides enhanced reliability in the LLC resonant converters.

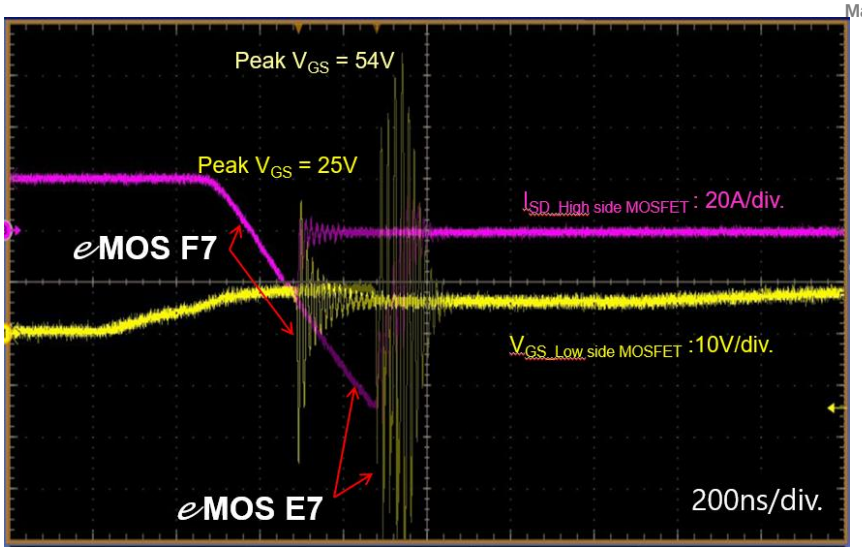


Figure 16. Reverse Recovery Characteristics of High Side MOSFET & Gate Oscillation of Low Side MOSFET during Reverse Recovery Operation of Body Diode

4. Conclusion

All the previously described key parameters are implemented in the design of eMOS F7 series to optimized for resonant topologies. Power Master Semiconductor's eMOS F7 series offers higher system efficiency and improved reliability for resonant topologies and bridge topologies for various applications.

5. 600V/650V eMOS F7/UF7 Product Portfolio & Nomenclature

5.1. 600V/650V eMOS F7/UF7 Product Portfolio

600V / 650V eMOS F7/UF7 Lineup

Battery Charger | PC Power | Audio | TV Power / LED | Server/Telecom Power | Solar Inverter | EV Charging Station | OBC

	PKG / $R_{DS(ON)\_max}$	Die	DPAK	PQFN88	TO-220	TO-220F	TO-247 3L
600V	30mΩ	**PMO60N030F7** (-A) *PMO60N030UF7 (-A)					**PMW60N030F7** (-A) *PMW60N030UF7 (-A)
	43mΩ	**PMO60N043F7** (-A) *PMO60N043UF7 (-A)					**PMW60N043F7** (-A) *PMW60N043UF7 (-A)
	75mΩ	**PMO60N075F7** (-A) *PMO60N075UF7 (-A)					**PMW60N075F7** (-A) *PMW60N075UF7 (-A)
	105mΩ	**PMO60N105F7** (-A) *PMO60N105UF7 (-A)					**PMW60N105F7** (-A) *PMW60N105UF7 (-A)
	193mΩ	**PMO60N193F7** (-A) *PMO60N193UF7 (-A)					
650V	43mΩ	*PMO65N043F7 (-A) *PMO65N043UF7 (-A)					**PMW65N043F7** (-A) *PMW65N043UF7 (-A)
	310mΩ	*PMO65N310F7 (-A) *PMO65N310UF7 (-A)				*PMF65N310F7 (-A) *PMF65N310UF7 (-A)	

* Coming Soon
(A- Automotive Grade)

Table 1. 600V/650V F7 eMOS Product Portfolio (UF7 : Ultra fast recovery super-junction MOSFET)

For more product information, please visit https://www.powermastersemi.com

5.2. Nomenclature

Device part number contains a lot of information such as technology, package, voltage rating and generation, etc. Figure 17 shows Power Master Semiconductor's super-junction MOSFET, eMOS nomenclature

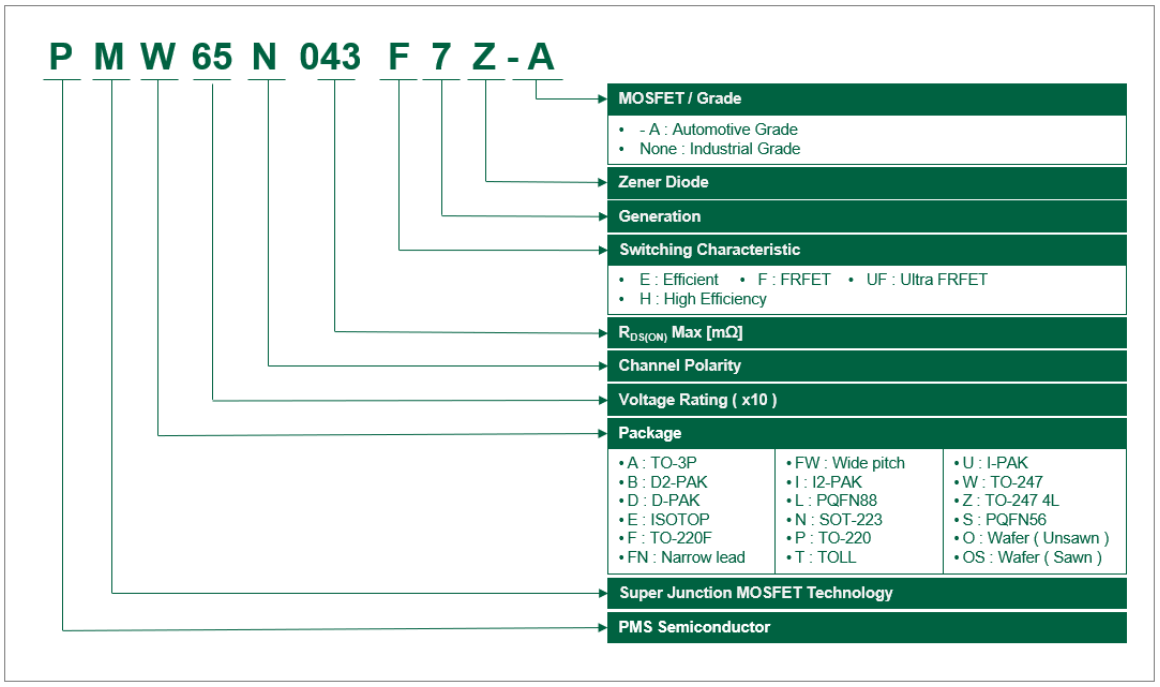


Figure 17. eMOS nomenclature scheme

6. Document Revision History

Major changes since the last version

Date	Description of change
19-January-2023	First Release

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